External Reliability Evaluation Report

New Resin Qualification on TO-92 package

General Information	
Product Lines	*BU 58*
Products Description	*TS110x* *XL0840x* *ACS10x* *P01x* *X0x* *Z0x* *FLC21-135A*
Product Group	*ADG*
Product division	*Discrete & Filter Division*
Package	*TO-92*
Maturity Step Level	***Qualified***

Locations	
Wafer fab	*STMicroelectronics Tours (FRANCE)*
Assembly plant	*Subcontractor 994X (CHINA)*
Reliability Lab	*STMicroelectronics Tours (FRANCE)*
Reliability assessment	***Pass***

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
Rev. 1	March 26th; 2019	11	Erika LAURET	Julien MICHELON	First issue

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD 22	Reliability test methods for packaged devices
JESD 47	Stress-Test-Driven Qualification of Integrated Circuits
JESD 94	Application specific qualification using knowledge based test methodology
MIL-STD-750C	Test method for semiconductor devices

2 GLOSSARY

BOM	Bill Of Materials
DUT	Device Under Test
HTRB	High Temperature Reverse Bias
TC	Temperature Cycling
THB	Temperature Humidity Bias
RSH	Resistance to Solder Heat
UHAST	Unbiased Highly Accelerated Stress Test
P/N	Part Number
RH	Relative Humidity
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

Qualification of new resin assembled in TO-92 package.

3.2 Conclusion

Qualification plan has been fulfilled without exception. Reliability tests have shown that those devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the robustness of those products and safe operation, which is consequently expected during their lifetime.

4 CHANGE DESCRIPTION

Qualification of new supplier of Halogen-Free Molding Compound for TO-92 package at subcontractor in China in replacement of current resin.

5 TESTS RESULTS SUMMARY

5.1 Test vehicles

Four test vehicles were chosen:

- ACS108-8TK-TR
- Z00607MA 1BA2
- P0102DA 5AL3
- TS110-8SA1

Lot #	Part number	Package	Comment
Lot 1	ACS108-8TK-TR	TO-92	Qualification data
Lot 2	Z00607MA 1BA2	TO-92	Qualification data
Lot 3	P0102DA 5AL3	TO-92	Qualification data
Lot 4	TS110-8SA1	TO-92	Qualification data

5.2 Test plan and results summary

Test	Std ref.	Conditions	SS	Step	Failure/SS			
					Lot 1	Lot 2	Lot 3	Lot 4
Die Oriented Tests								
HTRB	JESD22 A-108 MIL-STD-750C	Temperature=125°C Tension= VAC 600V	77	1000h		0/77		
HTRB	JESD22 A-108 MIL-STD-750C	Temperature=125°C Tension= VAC 800V	154	1000h	0/77			0/77
Package Oriented Tests								
TC	JESD22 A-104	Frequency (cy/h)=2cy/h Temperature (high)=150°C Temperature (low)=-65°C	308	500cy	0/77	0/77	0/77	0/77
RSH	ST 0060102 JESD22 B-106-A	Temperature=260°C Time (on)=10s	30	MESURE AFTER DIP			0/30	
THB	JESD22 A-101	Humidity (HR)=85% Temperature=85°C Tension=100V	74	1000h	0/25	0/25		0/24*
UHAST	JESD22 A-118	Humidity (HR)=85% Pressure=2.3bar Temperature=130°C	231	96h	0/77	0/77		0/77

* Note: quantity reduced due to scrap unit

6 ANNEXES

6.1 Device details

6.1.1 Pin connection

Refer to products datasheets.

6.1.2 Package outline/Mechanical data

Refer to products datasheets

6.2 Tests Description

Test name	Standard Reference	Description	Purpose
Die Oriented			
HTRB High Temperature Reverse Bias	JESD22 A-108 MIL-STD-750C	HTRB : High Temperature Reverse Bias HTFB / HTGB : High Temperature Forward (Gate) Bias. The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: - low power dissipation; - max. supply voltage compatible with diffusion process and internal circuitry limitations.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
Package Oriented			
TC Temperature Cycling	JESD22 A-104	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	JESD22 A-101	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
RSH Resistance to solder heat	ST 0060102 JESD22 B-106-A	Device is submitted to a dipping in a solder bath at 260°C with a dwell time of 10s. Only for through hole mounted devices.	This test is used to determine whether solid state devices can withstand the effects of the temperature to which they will be subjected during soldering of their leads. The heat is conducted through the leads into the device package from solder heat at the reverse side of the board. This procedure does not simulate wave soldering or reflow heat exposure on the same side of the board as the package body.
UHAST Unbiased Highly Accelerated Stress Test	JESD22 A-118	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.

6.3 List of product involved in this qualification

X00602MA 1AA2	P0102DA 5AL3
X00602MA 2AL2	P0109DA 5AL3
X00602MA 5AL2	P0111DA 1AA3
X00619MA1AA2	P0111DA 5AL3
X00619MA2AL2	P0111MA 1AA3
X00619MA5AL2	P0111MA 1AA3
X0202DA 1BA2	P0111MA 1AA3
X0202MA 1BA2	P0115DA 5AL3
X0202MA 2BL2	P0115DA 5AL3
X0202NA 1BA2	P0118DA 1AA3
X0202NA2BL2	P0118DA 1AA3
X0203MA 1BA2	P0118MA 2AL3
X0203NA 1BA2	P0118MA 5AL3
X0205MA 1BA2	P0124CA 5AL3
X0205MA 2BL2	P0130AA 1EA3
X0205NA 1BA2	P0130AA 2AL3
X0225MA 1DA2	ACS102-6TA-TR
X0227MA 5DL2	FLC21-135A
Z00607MA 1BA2	XL0840
Z00607MA 2BL2	XL0840-AP
Z00607MA 5BL2	XL0840-TR
Z0103MA 1AA2	ACS108-6SA
Z0103MA 2AL2	ACS108-6SA-AP
Z0103MA 5AL2	ACS108-6SA-TR
Z0103NA 1AA2	ACS108-8SA
Z0103NA 2AL2	ACS108-8SA-AP
Z0107DA 2AL2	ACS108-8SA-TR
Z0107MA 1AA2	TS110-7A1
Z0107MA 2AL2	TS110-7A1-AP
Z0107MA 5AL2	TS110-8A1
Z0107NA 1AA2	TS110-8A1-AP
Z0107NA 2AL2	TS110-8A2
Z0107NA 5AL2	TS110-8A2-AP
Z0109MA 1AA2	TS110-8SA1
Z0109MA 2AL2	TS110-8SA1-AP
Z0109MA 5AL2	TS110-8SA2
Z0109NA 2AL2	TS110-8SA2-AP
Z0110MA 1AA2	
Z0127MA 2EL2	
P0102DA 1AA3	
P0102DA 2AL3	

AMG (Analog & MEMS Group)
General Purpose Analog & RF Division
Signal Conditioning& Interface

REL.6088-686-19W

Quality and Reliability

Reliability Evaluation Report

QUALIFICATION of NEW RESIN on TO92

ASE WEIHAI

General Information	
Product Lines	*TV1: LA05* *TV2: S431*
Product Description	Positive voltage regulators LOW Voltage Adjustable Shunt Reference Low current 1.2 to 37 V adjustable
P/N Positive voltage regulators	*TV1: L78L05* *TV2:TS431*
Product Group	*AMG*
Product division	*General Purpose Analog & RF Division*
Package	*TO92*
Silicon Process technology	*TV1:HBIP40V* *TV2:HF2CMOS*

Locations	
Wafer fab	*Singapore 6*
Assembly plant	*ASE WEIHAI*
Reliability Lab	*Catania Reliability LAB*

DOCUMENT INFORMATION

Version	Date	Pages	Handled by	Comment
1	June 2019	7	Antonio Russo Giuseppe Giacopello	Final Report

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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits
Report ID: 19032QRP	New Resin Qualification on TO-92 package (ADG)

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW OBJECTIVES

In order to qualify new molding compound for TO92 assembled in ASE Weihai, three assy lot are requested. We have performed reliability trials on two TVs adding ADG reliability data (as 3nd assy lot, Report ID: 19032QRP)

4 CONCLUSION

Qualification plan has been fulfilled without exception. Reliability tests have shown that those devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the robustness of those products and safe operation, which is consequently expected during their lifetime.

5 DEVICE CHARACTERISTIC

5.1 Change description

Qualification of new supplier of Halogen-Free Molding Compound for TO-92 package at subcontractor in China in replacement of current resin.

5.2 Construction note

P/N	L78L05	TS431
Wafer/Die fab. information		
Wafer fab manufacturing location	Ang Mo Kio 6”	
Technology	HBIP40V	HF2CMOS
Die finishing back side	Lapped Silicon	
Die size	0.706X0.766	0.900X1.350
Passivation type	SiN (nitride)	
Wafer Testing (EWS) information		
Electrical testing manufacturing location	Ang Mo Kio EWS	
Tester	ASL1000	
Test program	LA78L05-MS02.nX4	S431 TS431.5
Assembly information		
Assemby Site	ASE WEIHAI	
Package description	TO 92	
Molding compound	Epoxy	
Frame	WSD-0200 TO-237	
Die attach material	Epoxy	
Wires bonding materials/diameters	Cu 1mil	Gold 1mil
Final testing information		
Testing location	ASE WEIHAI	
Tester	ASL1000	
Test program	LA78L05-MS02.nX4	S431 TS431.5

6 TEST VEHICLE & TEST PLAN

Lot #	T.V.	Process/ Package	Product Line	Comments
1	L78L05ABZ-AP	TO92	LA0501	
2	TS431IZT		S43101	

Test	PC	Std ref.	Conditions	SS	Steps h=hours cy=cycles	Failure/SS		Note
						L7805	TS431	
Die Oriented Tests								
HTOL		JESD22 A-108	Ta=125°C Vbias= 5V	77	168 h		0/77	
					500 h		0/77	
					1000 h		0/77	
HTOL		JESD22 A-108	Ta=125°C Vbias= 35V	77	168 h	0/77		
					500 h	0/77		
					1000 h	0/77		
HTSL		JESD22 A-103	Ta=150°C	154	168 h	0/77	0/77	
					500 h	0/77	0/77	
					1000 h	0/77	0/77	
Package Oriented Tests								
THB		JESD22 A-101	Ta = 85°C, RH=85%, BIAS +24V	50	168 h	0/25	0/25	
					500 h	0/25	0/25	
					1000 h	0/25	0/25	
TC		JESD22 A-104	Ta = -65°C to +150°C	154	100 cy	0/77	0/77	
					500 cy	0/77	0/77	
					1000 cy	0/77	0/77	
AC		JESD22 A-102	Pa=2Atm / Ta=121°C	154	96 h	0/77	0/77	

NOTE: For the 3nd lot Reliability data, please refer to ADG Report ID: 19032QRP

7 ANNEXES

7.1 Devices details

7.1.1 Pin connections

Refer to products datasheet

7.1.2 Package Mechanical data

Refer to products datasheet

8 TEST DESCRIPTION

Test name	Description	Purpose
Die Oriented		
HTOL High Temperature Operative Life	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
Package Oriented		
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.